Solid State Transformers: Benefits and Challenges

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BACKGROUND: FUTURE SMART GRIDS

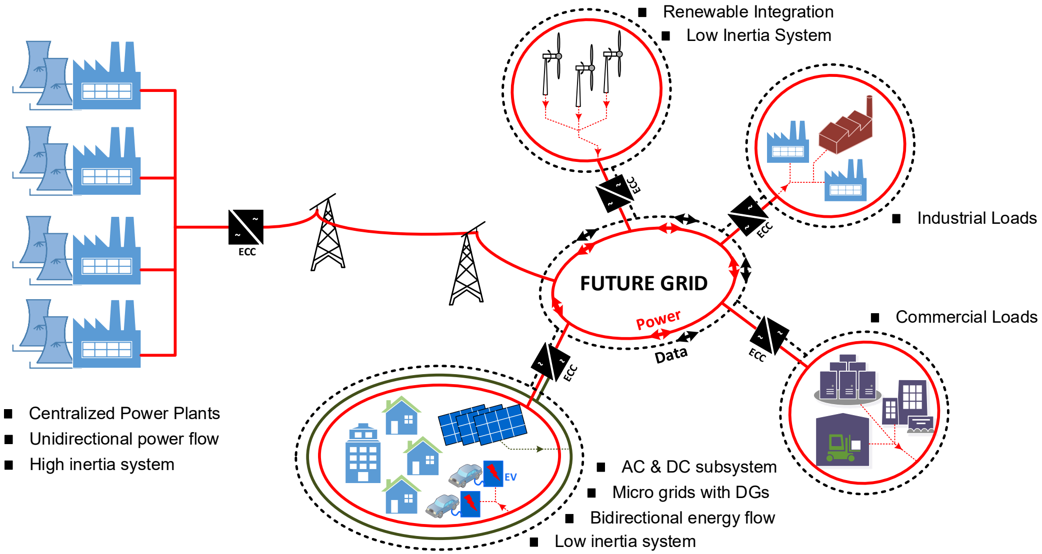


Fig. A possible Illustration of future grid

FUTURE SMART GRID

- ❑ **High penetration** of distributed energy resources (DER) and energy storage (DES)
- ❑ **Sizable dynamic power** consumers (e.g. EV loads)
- ❑ **Bidirectional power** flow
- ❑ **Communication layer** to enable critical information exchange

- Conventional power grid has line-frequency **(LF) transformers (LFT) + on-load tap changers** to connect sizable loads to the grid.
- **LFT with on-load tap changers can under-perform in future grid** especially due to penetration of highly intermittent DERs, fast switching (synchronized/islanded) and constant power loads.
- LFT in conventional power grids are **replaced by energy control centers** (ECC) in future grid.

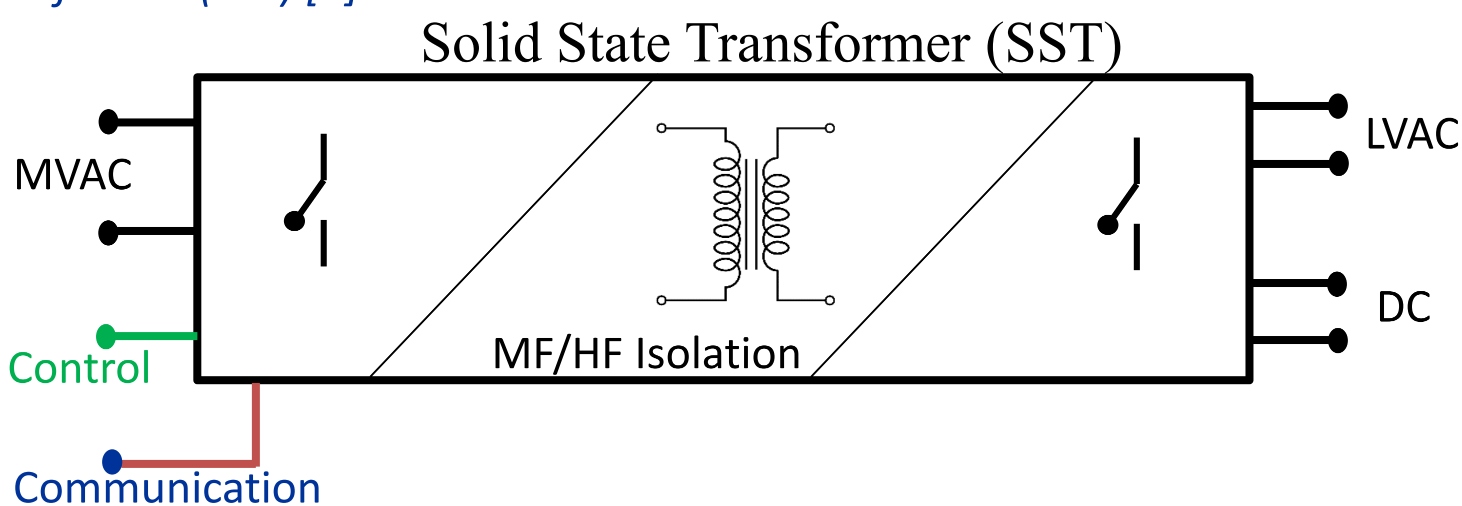
BACKGROUND: SOLID STATE TRANSFORMER

Basic functionalities of ECC -

- Controlled active power flow
- Required ancillary services
- Information exchange
- Synchronous/asynchronous operation
- Regulated DC bus

A suitable candidate to realize ECC is **Solid State Transformer (SST)**

Definition: *A power electronic system acting as an interface between an MV and a LV system with medium-frequency (MF) or high-frequency (HF) isolation stages and providing a control input and/or a communication port and a DC port is commonly named as solid-state transformer (SST) [1]*



1. D. Rothmund, G. Ortiz, T. Guillod, and J. Kolar, "10kv sic-based isolated dc-dc converter for medium voltage-connected solid-state transformers," in 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 1096–1103, IEEE, 2015.

BACKGROUND: LFT AND SST

Conventional Transformers [1]

- Robust and reliable
- High-efficiency > 99%
- Control of power flow: Not possible
- DC sub-system: Not possible
- Low frequency isolation: Bulky

Solid State Transformer [2]

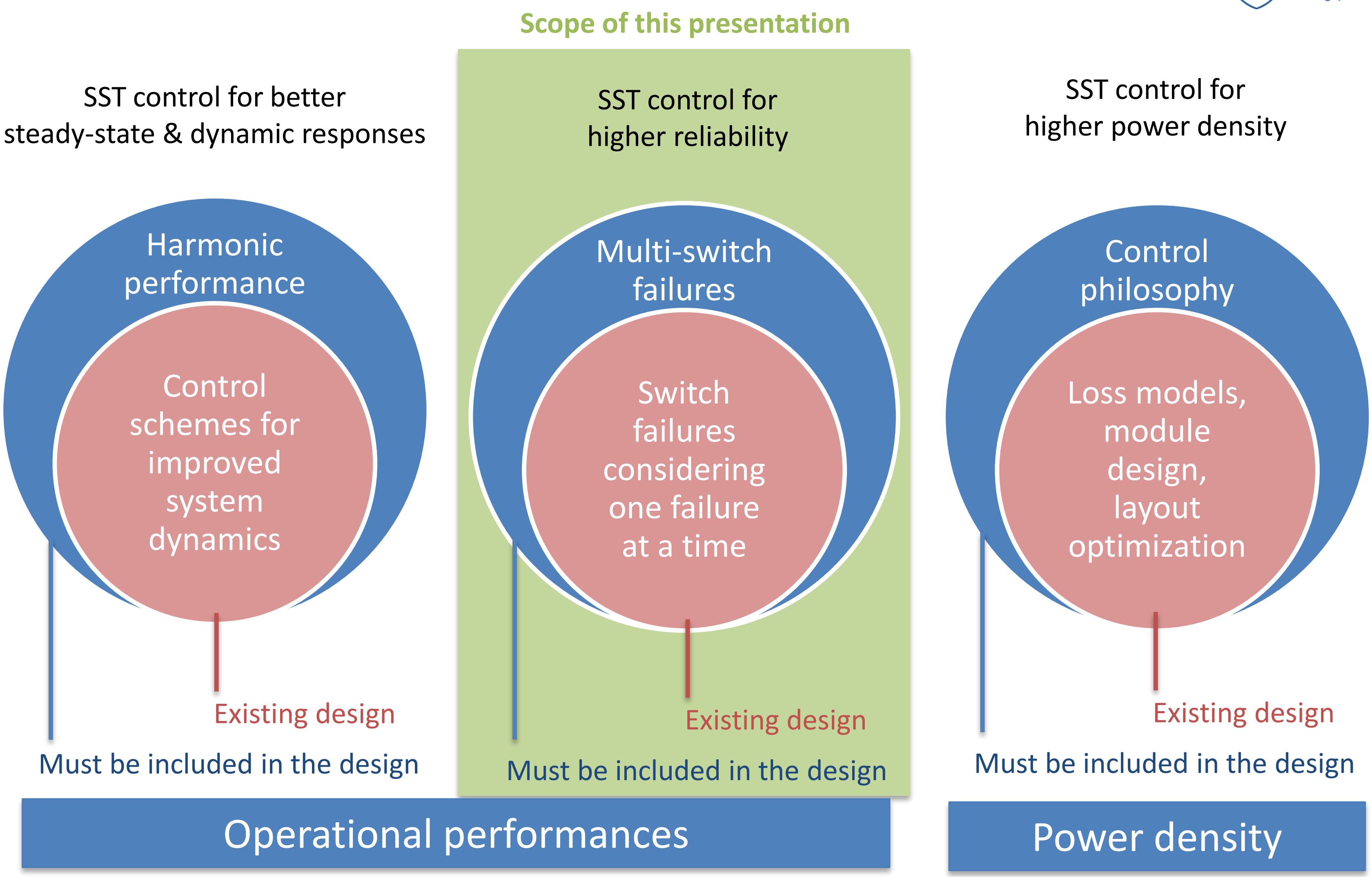
VS

- Reliability and robustness: Control
- Control of power and information: Possible
- DC and AC sub-systems: Possible
- Medium/high frequency isolation: Less bulky

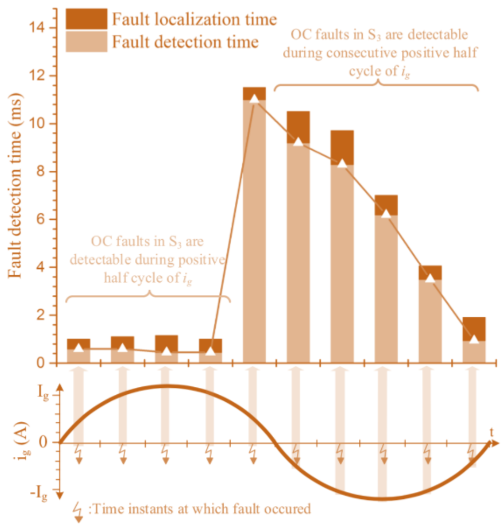
1 http://www.gobizkorea.com/Distribution_Power_Transformer_cid080114010000

2. D. Dujic, C. Zhao, A. Mester, J. K. Steinke, M. Weiss, S. Lwedeni-Schmid, T. Chaudhuri, and P. Stefanutti, "Power Electronic Traction Transformer—Low Voltage Prototype," IEEE Trans. Power Electron., vol 28, no. 12, Dec. 2013

CHALLENGES IN SST

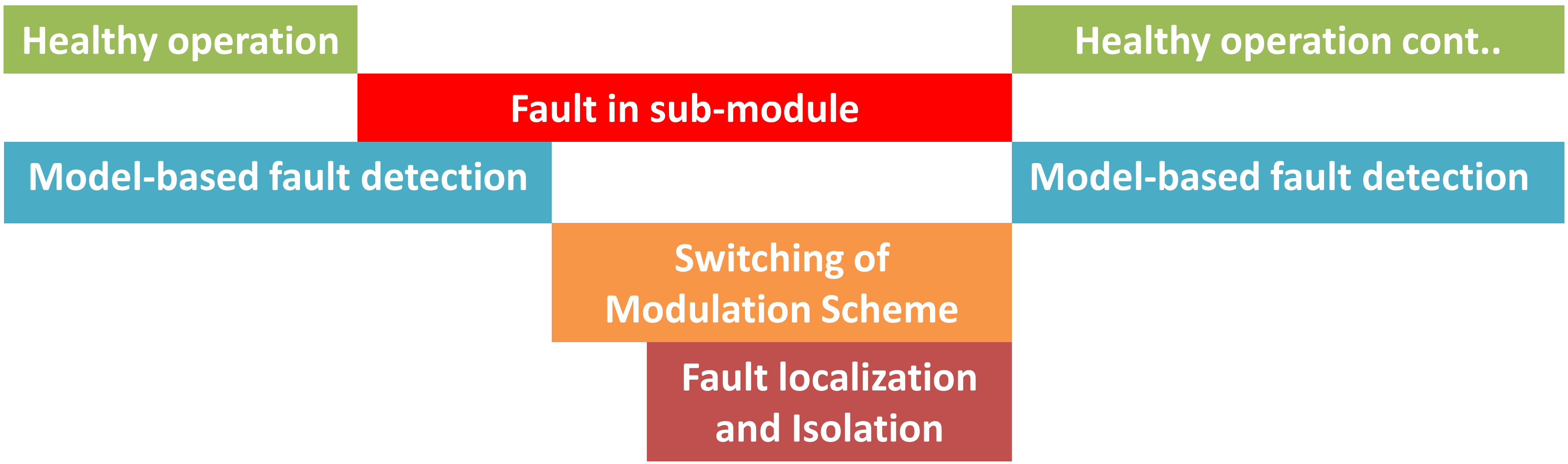


FAULT DETECTION, LOCALIZATION AND ISOLATION (FDLI) IN SOLID STATE TRANSFORMER

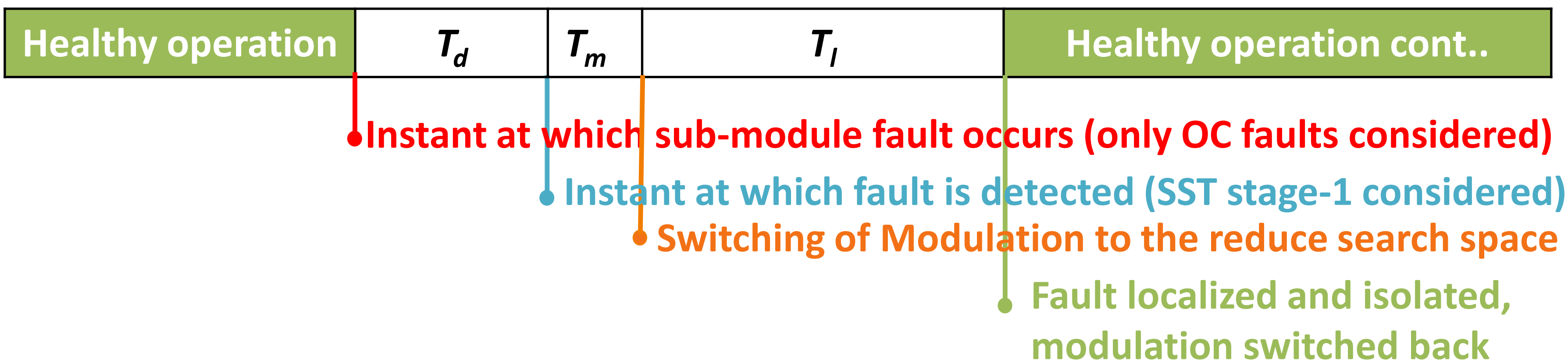


NEW MODEL-BASED FDLI: OVERVIEW

SEQUENCE OF OPERATIONS IN SST



TIME FOR VARIOUS OPERATIONS



NEW MODEL-BASED FDLI: VALIDATION

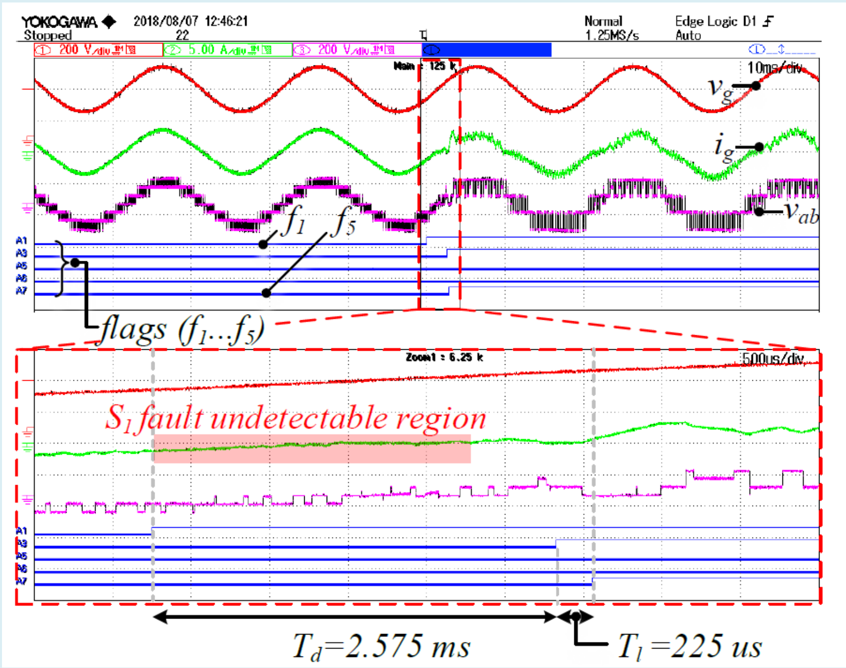


Illustration of fault detection and localization time for single switch failure in single module case

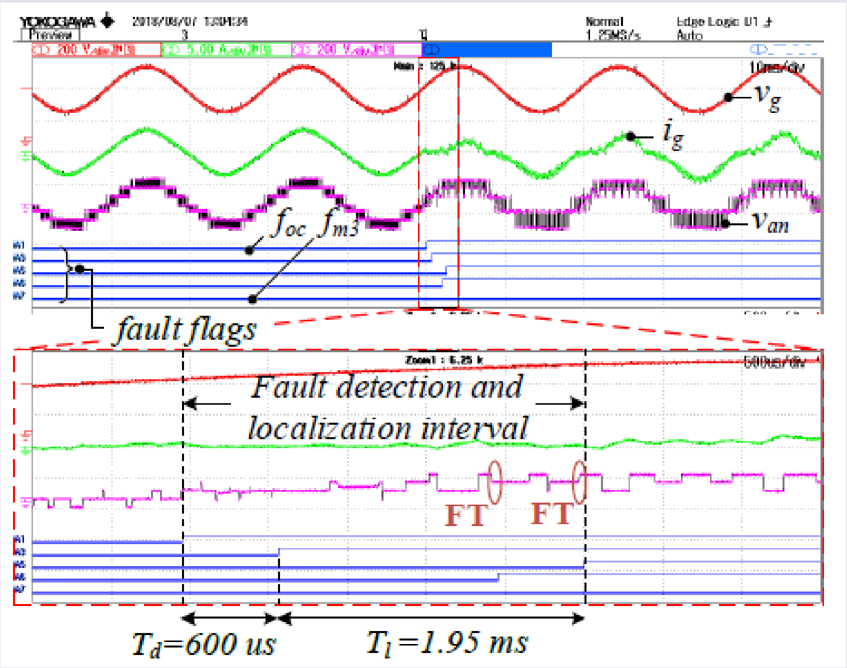
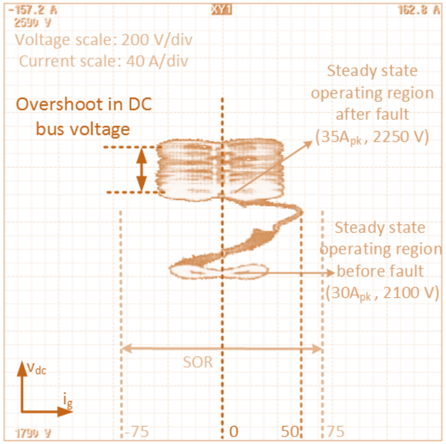


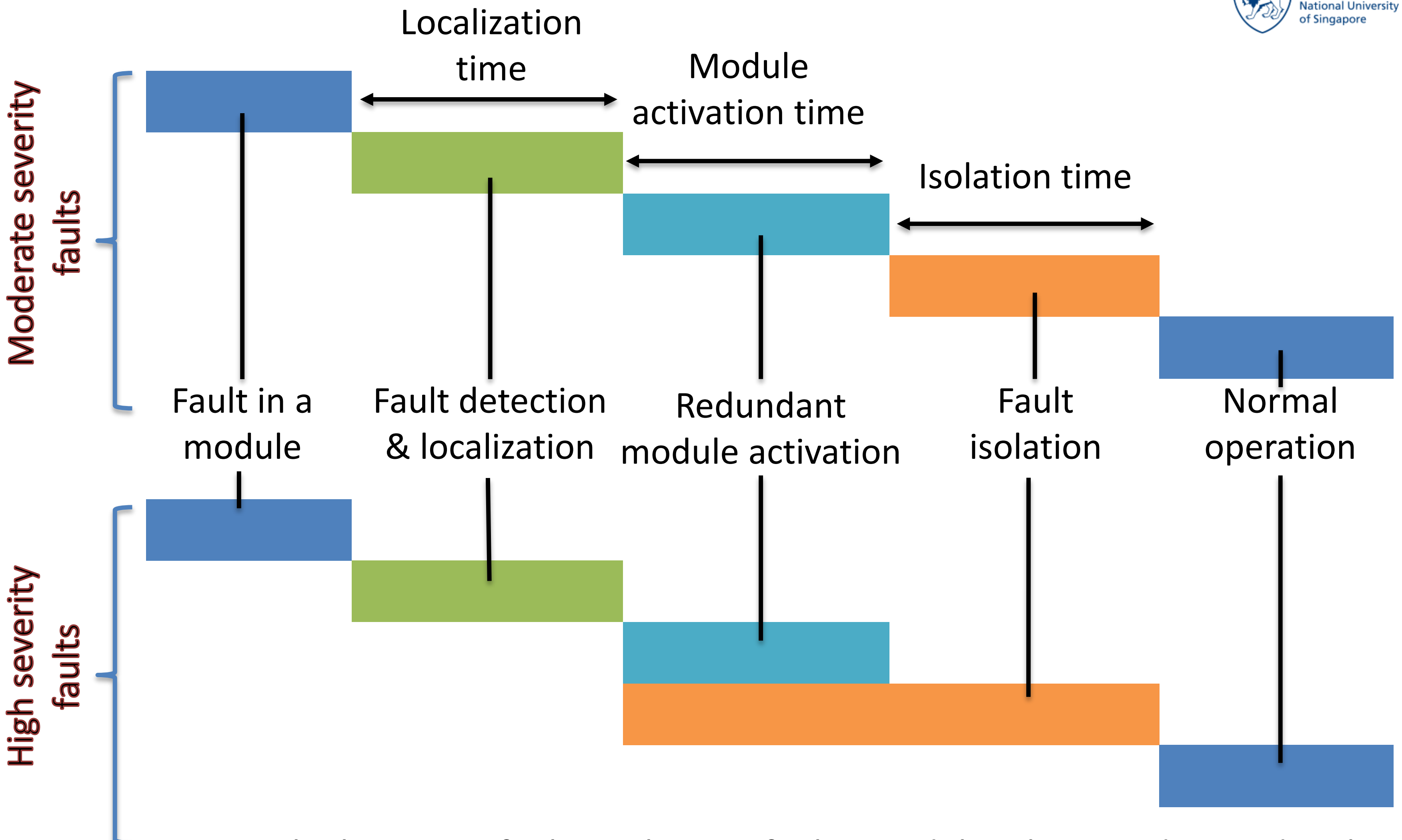
Illustration of fault detection and localization time for simultaneous multi-switch failure in multiple modules case

Worst case scenario: Time for fault detection + fault localization < 20 *ms (one fundamental line cycle)*

POST-FAULT RESTORATION SCHEME FOR SOLID STATE TRANSFORMER



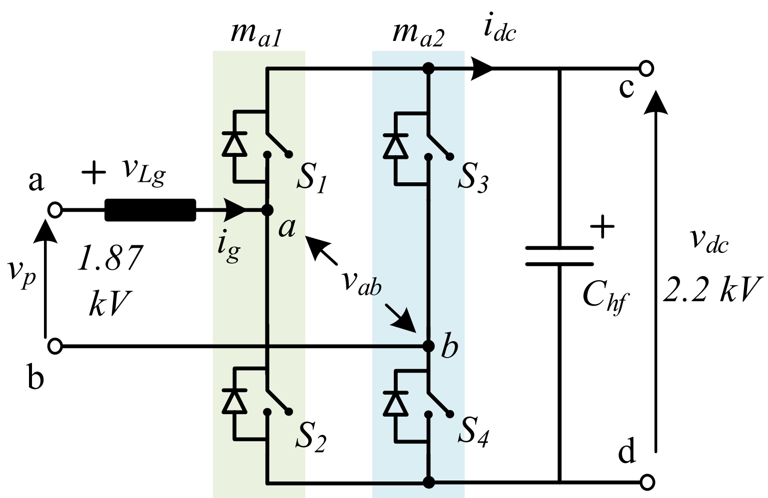
POST-FAULT RESTORATION SCHEME

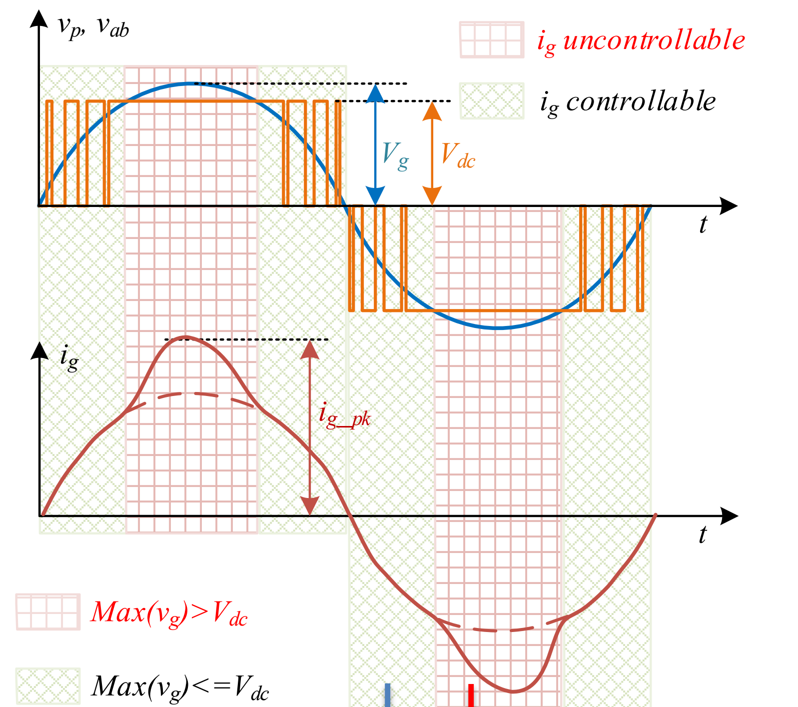


For high severity faults such as SC faults, module is bypassed immediately

INDUCTOR CURRENT REGULATION

1-ph boost rectifier



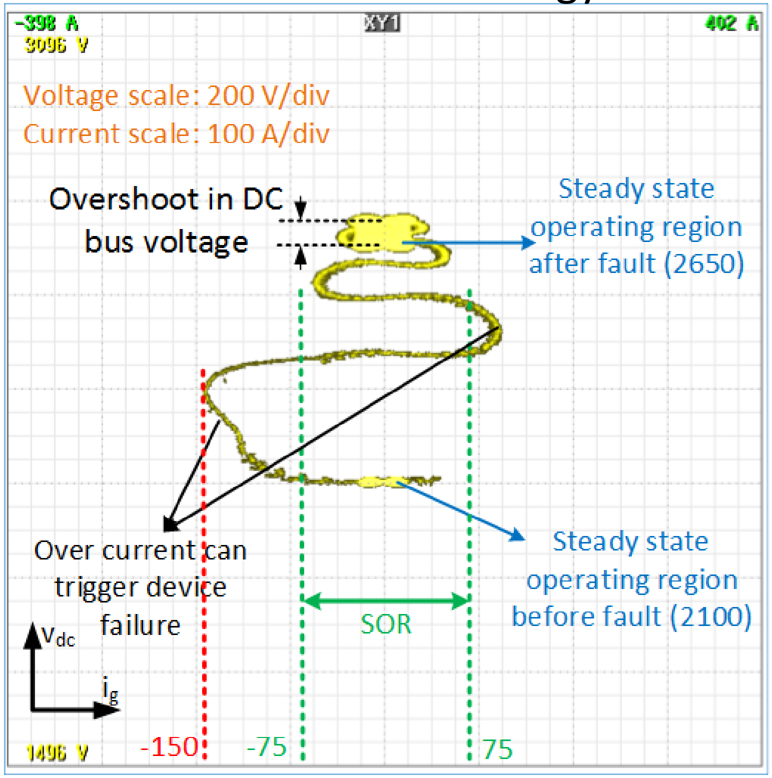


- Scenario happens when one of the modules is bypassed without an active redundant module
- Control scheme to regulate grid current during these conditions is necessary to avoid cascading failures

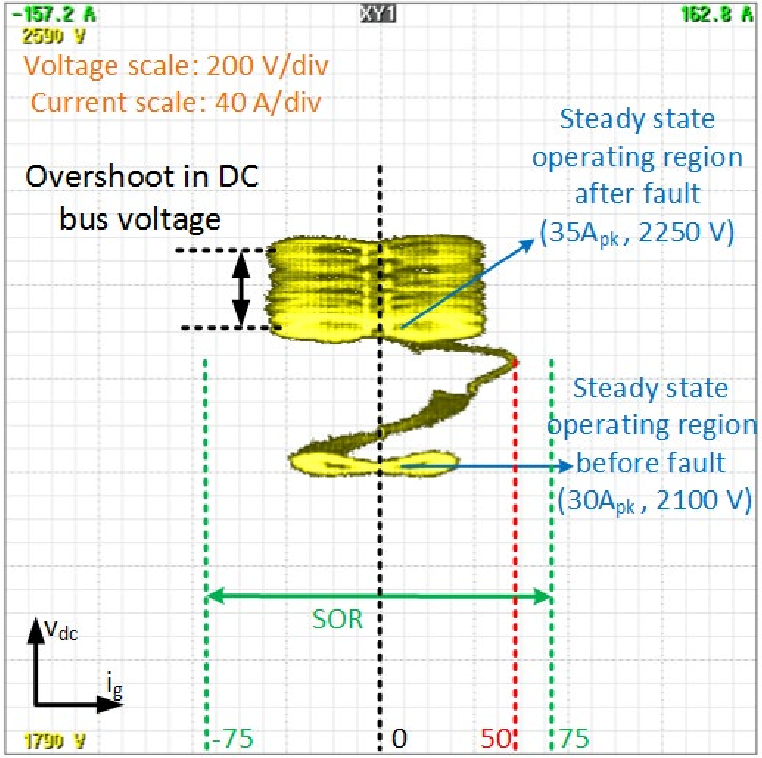
Full control over i_g No control over i_g

PROPOSED POST-FAULT RESTORATION:

Conventional Strategy



Proposed Strategy



<u>After fault:</u>

DC bus voltage: 2650 V

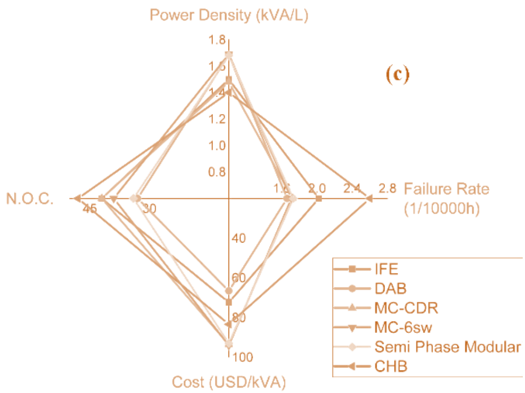
Peak current: 150 A

<u>After fault:</u>

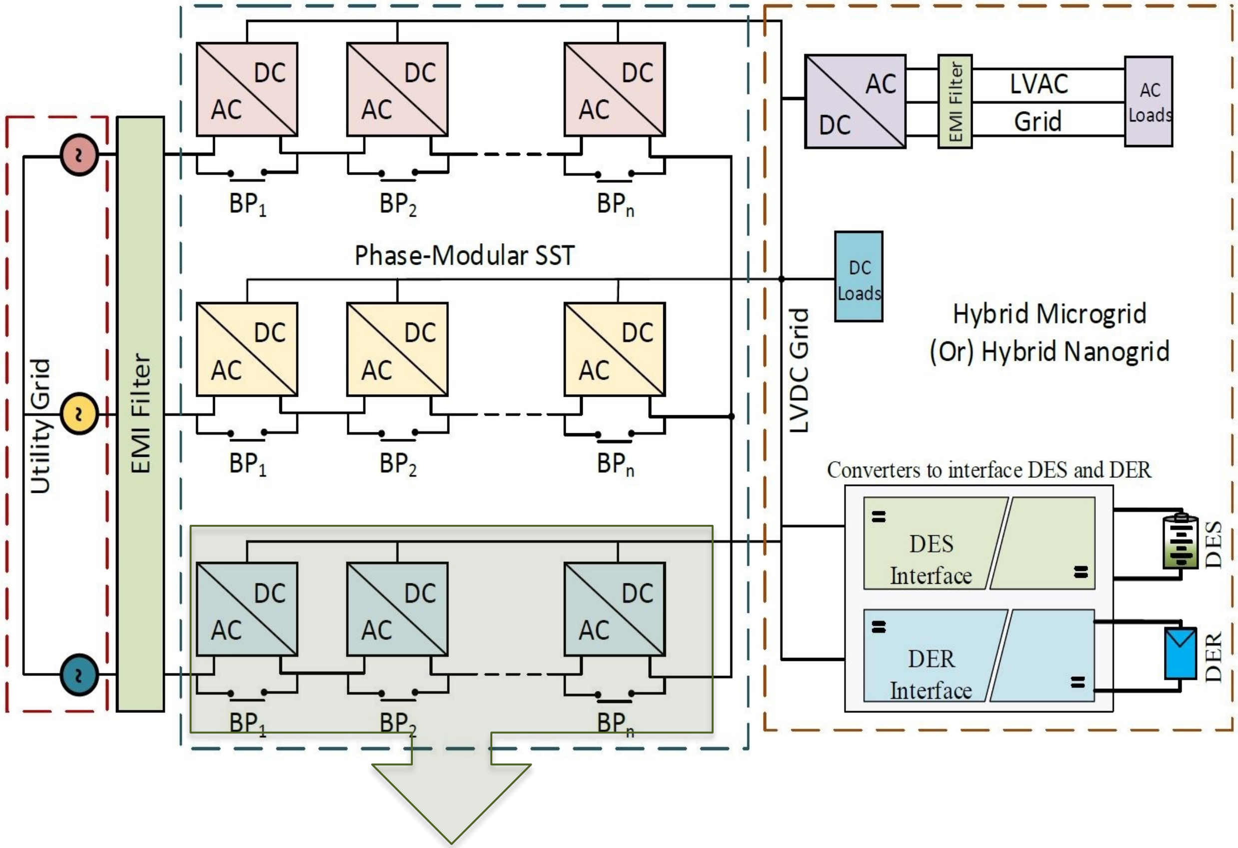
DC bus voltage: 2250 V

Peak current: 50 A

SCOPE FOR ADVANCED SST TOPOLOGIES



SCOPE FOR ADVANCED TOPOLOGIES



Conventional SST

Est. power density: 1.7 kW/L

Est. Cost – 80 USD/kVA

Est. failure rate – $2.6\text{X}10^{-4}$/hr

Matrix-based SST

Est. power density: 1.685 kW/L

Est. Cost – 66.6 USD/kVA

Est. failure rate – $1.66\text{X}10^{-4}$/hr

- Modular architecture (Matrix based AC-DC stage)
- Single-stage AC-DC power conversion → improved efficiency and power density

MATRIX BASED AC-DC TOPOLOGIES

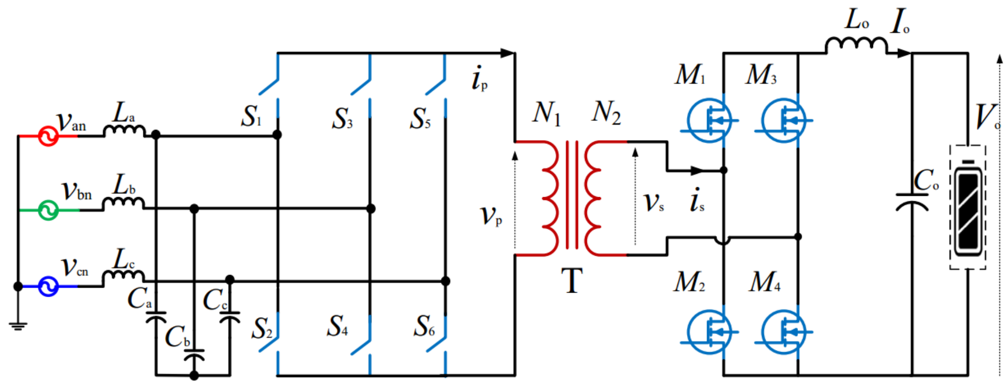
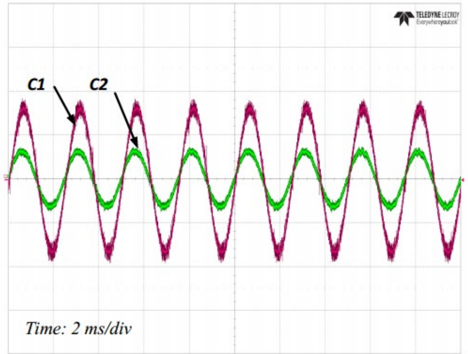


Fig. 3-ph AC-DC matrix-based power converter for battery charging applications. (EMA funded Project)



C1: phase-a voltage, v_{an} (100 V/div), C2: Input phase-a current, ia (4 A/div).

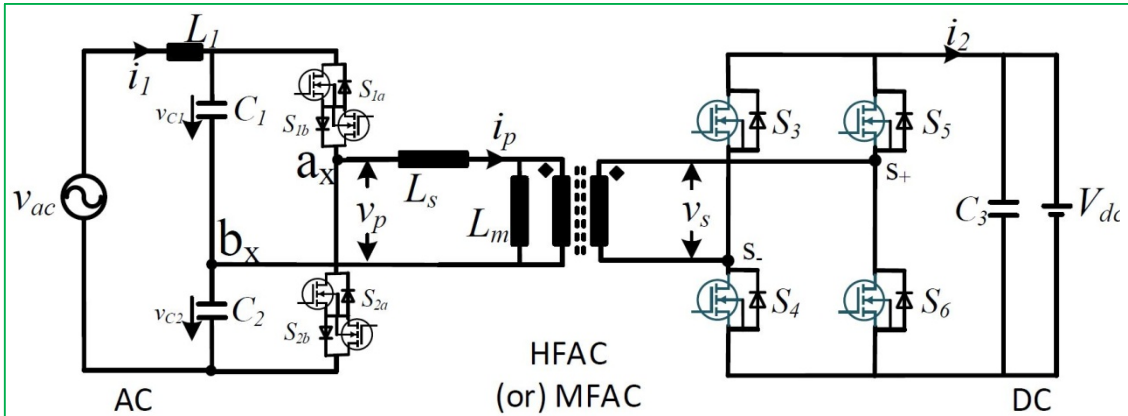
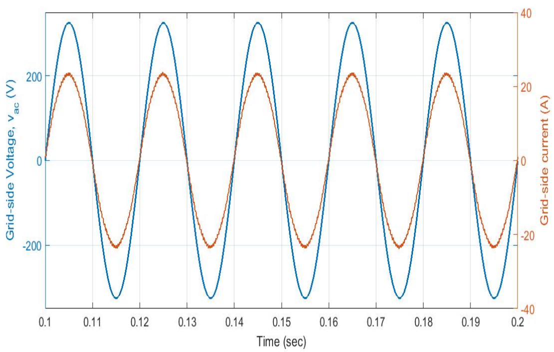
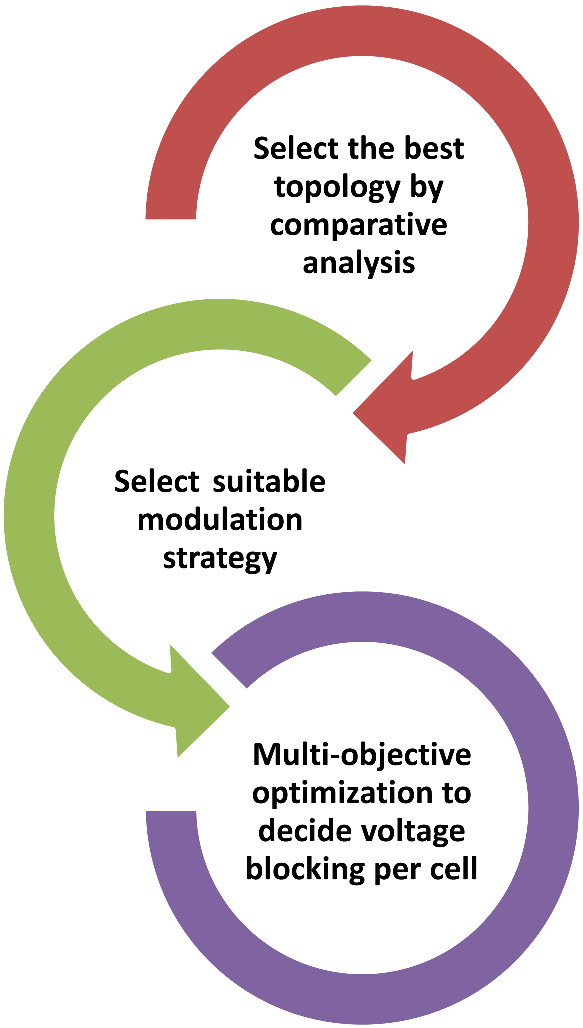


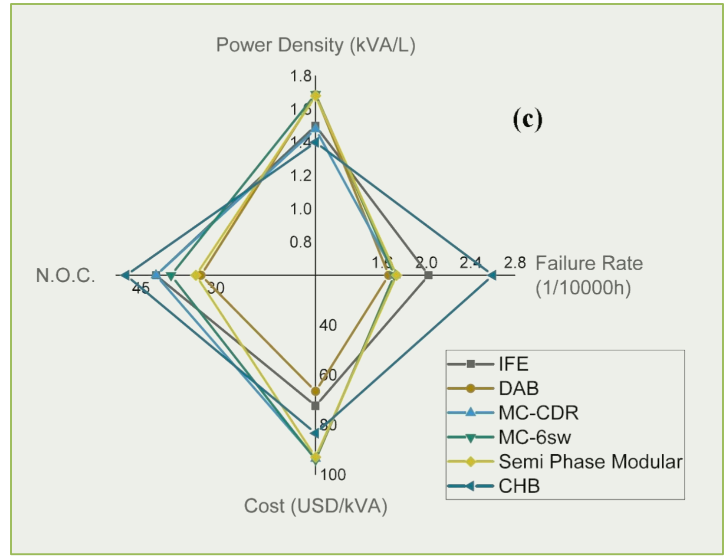
Fig. 1-ph AC-DC matrix-based power converter for SST applications



Simulated grid current with THD < 5%

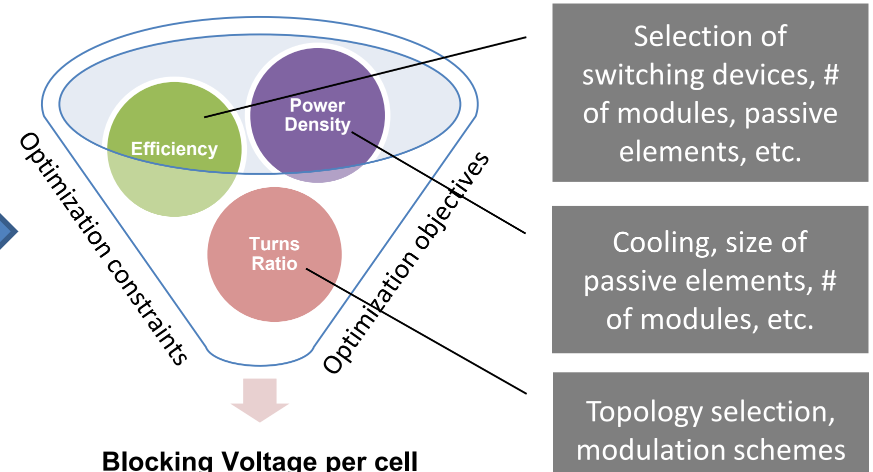
TOPOLOGIES SELECTION





A study of various SST topologies (possible + proposed in literature) to estimate power density, cost and reliability.

Models considered for this study are taken from the literature and accuracy of predictions are subjected to the model accuracy.



CONCLUSIONS

- SST is proposed as a possible replacement to conventional transformer in future power grid.
- As an all silicon-based solution, SSTs are most prone to failures due to dynamic grid conditions.
- Mechanisms to detect failures (both open-circuit and short-circuit) is a must.
- Control during post-fault restoration is necessary to avoid cascading failures especially for grid applications.
- Plenty of scope for further improving the power density and cost → Advanced topologies

PUBLICATIONS AND REFERENCES

Journals

1. *Naga Brahmendra Yadav Gorla, S. Kolluri, M. Chai and S. K. Panda, "A Comprehensive Harmonic Analysis and Control Strategy for Improved Input Power Quality in a Cascaded Modular Solid State Transformer," in IEEE Transactions on Power Electronics, vol. 34, no. 7, pp. 6219-6232, July 2019.*
2. *Naga Brahmendra Yadav Gorla, S. Kolluri, M. Chai and S. K. Panda, "A Novel Open Circuit Fault Detection and Localization for Cascaded H-bridge Stage of a Three-stage Solid State Transformer ," in IEEE Transactions on Power Electronics (early accesses).*
3. *M. Chai, Naga Brahmendra Yadav Gorla and S. K. Panda, "Improved Performance With Dual-Model Predictive Control for Cascaded H-Bridge Multilevel Converter," in IEEE Transactions on Industry Applications, vol. 55, no. 5, pp. 4886-4899, Sept.-Oct. 2019.*

Conferences

1. *Naga Brahmendra Yadav Gorla, S. Kolluri and S. K. Panda, "Solid state transformer control aspects for various smart grid scenarios," 2017 IEEE Innovative Smart Grid Technologies - Asia (ISGT-Asia), Auckland, 2017, pp. 1-6.*
2. *Naga Brahmendra Yadav Gorla, S. Kolluri, M. Chai and S. K. Panda, "A New Control Scheme to Process Ripple Power Through Isolation stage of the Three-stage Solid State Transformer,", accepted for presentation in IEEE ICPE-2019 ECCE Asia.*
3. *Naga Brahmendra Yadav Gorla, S. Kolluri, P. Das and S. K. Panda, "A new control scheme to improve load transient response of single phase PWM rectifier with Auxiliary Current Injection Circuit," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 552-557.*
4. *Naga Brahmendra Yadav Gorla, K. Ali, P. Das and S. K. Panda, "Analysis of active power decoupling in single-phase rectifier using six-switch topology," 2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC), Auckland, 2016, pp. 1-6.*
5. *Naga Brahmendra Yadav Gorla, S. Kolluri, M. Chai and S. K. Panda, "A New Open-circuit Fault Detection and Localization Scheme for Cascaded H-Bridge Multilevel Converter," accepted in IEEE INTELEC 2019.*
6. *Naga Brahmendra Yadav Gorla, S. Kolluri, P. J. Chauhan and S. K. Panda, "A fault tolerant control approach for a three-stage cascaded multilevel solid state transformer," 2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL), Stanford, CA, 2017, pp. 1-6.*
7. *Naga Brahmendra Yadav Gorla, K. Ali, C. C. Lin and S. K. Panda, "Improved utilization of grid connected voltage source converters in smart grid through local VAR compensation," IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society, Yokohama, 2015, pp. 002532-002537.*
8. *J. Saha, Naga Brahmendra Yadav Gorla and S. K. Panda, "A Matrix-Based Solid-State-Transformer For A Hybrid Nanogrid," 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Chennai, India, 2018, pp. 1-6.*
9. *M. Chai, Naga Brahmendra Yadav Gorla and S. K. Panda, "Dual-Model Predictive Control for Cascaded H-Bridge Multilevel Active Rectifier with DC Voltage Balancing in a Solid-State Transformer," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 5657-5663.*
10. *J. Saha, Naga Brahmendra Yadav Gorla and S. K. Panda, "A Review on Matrix-Based Bidirectional AC-DC Conversion for Modular SSTs" accepted for presentation in INTELEC 2019.*

Patents

1. *Jaydeep saha, National university of Singapore 2019, A Matrix Based Solid State Transformer for a Hybrid Nano grid, 10201811326W.*

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